What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A CMOS imager having improved transistor speed comprising:

a substrate;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region and at least one transistor wherein said transistor includes an opaque conductive layer deposited over the gate region of said transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

2. The CMOS imager according to claim 1, wherein said photo-collection region includes a photogate.

3. The CMOS imager according to claim 1, wherein said opaque conductive layer is an opaque conductive silicide layer.

4. The CMOS imager according to claim 1, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

5. The CMOS imager according to claim 3, wherein said opaque conductive silicide layer is a tungsten silicide.

6. The CMOS imager according to claim 3, wherein said opaque conductive silicide layer is a titanium silicide.

7. The CMOS imager according to claim 3, wherein said opaque conductive silicide layer is a cobalt silicide.

8. The CMOS imager according to claim 3, wherein said opaque conductive silicide layer is a molybdenum silicide.

9. The CMOS imager according to claim 4, wherein said opaque conductive barrier metal layer is a TiN/W layer.

10. The CMOS imager according to claim 4, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

11. The CMOS imager according to claim 4, wherein said opaque conductive barrier metal layer is a WN_x layer.

12. The CMOS imager according to claim 1, wherein said transistor is one or more of a reset transistor, a row select transistor, source follower transistor, amplifier transistor or a transfer transistor

13. The CMOS imager according to claim 1, wherein said transistor is a reset transistor.

14. The CMOS imager according to claim 13, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing

circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

15. The CMOS imager according to claim 1, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

16. The CMOS imager according to claim 15, wherein said imager further includes a light shield formed over said imager such that said light shield does not cover a substantial portion of said photocollection region.

17. A method of forming a CMOS imager, comprising the steps of:

forming an insulating layer over a semiconductor substrate having a photo-collection region;

forming at least one transistor gate over a portion of said insulating layer;

forming an opaque conductive layer over said photo-collection region, said at least one transistor gate and said insulating layer; and

selectively removing said opaque conductive layer from said insulating layer and said photo-collection region.

18. The method according to claim 17, wherein said photo-collection region includes a photogate.

19. The method according to claim 17, wherein said transistor gate includes a reset gate.

20. The method according to claim 19, further comprising a transfer gate.

21. The method according to claim 17, wherein said transistor gate includes an amplifying transistor.

22. The method according to claim 21, wherein said amplifying transistor is a source follower transistor.

23. The method according to claim 20, further comprising a row select gate.

24. The method according to claim 20, wherein said transfer gate and said reset gate are formed by depositing a doped polysilicon and selectively removing portions of said doped polysilicon to form transistor gates.

25. The method according to claim 24, wherein said doped polysilicon is selectively removed by etching.

26. The method according to claim 17, wherein said insulating layer is a silicon dioxide.

27. The method according to claim 26, wherein said insulating layer is deposited by thermal oxidation of silicon.

36. The method according to claim 29, wherein said opaque conductive barrier metal layer is a WN_x layer.

37. The method according to claim 28, wherein said opaque conductive layer silicide layer is deposited by chemical vapor deposition.

38. The method according to claim 28, wherein said opaque conductive layer silicide layer is deposited by sputtering.

39. The method according to claim 29, wherein said opaque conductive barrier layer is deposited by chemical vapor deposition.

40. The method according to claim 29, wherein said opaque conductive barrier layer is deposited by sputtering.

41. The method according to claim 17, wherein said opaque conductive layer is selectively removed by etching.

42. The method according to claim 17, wherein a ring portion of opaque conductive layer remains over an outer periphery of said photo-collection region.

43. The method according to claim 42, further including adding a light shield over a portion of said imager.

44. A method of forming a CMOS imager, comprising the steps of:

forming an insulating layer over a semiconductor substrate having a doped photocollection region;

depositing a doped polysilicon layer over said insulating layer;

depositing a photocollection insulator over said photocollection region;

forming an opaque conductive layer over said doped polysilicon layer; and

patterning said imager to form at least one gate stack having said opaque conductive layer over said gate stack.

45. The method according to claim 44, wherein said photo-collection region includes a photogate.

46. The method according to claim 44, wherein said transistor gate stacks include a reset gate.

47. The method according to claim 46, further comprising a transfer gate stack.

48. The method according to claim 47, further comprising a row select gate stack.

49. The method according to claim 44, wherein said transistor gates include an amplifying transistor gate stack.

50. The method according to claim 49, wherein said amplifying transistor is a source follower transistor gate stack.

51. The method according to claim 47, wherein said transfer gate and said reset gate are formed by depositing a mask and resist and selectively removing a portion of said opaque conductive layer, said doped polysilicon layer to form transistor gates.

52. The method according to claim 51, wherein said layers are selectively removed by etching.

53. The method according to claim 44, wherein said insulating layer is a silicon dioxide.

54. The method according to claim 53, wherein said insulating layer is deposited by thermal oxidation of silicon.

55. The method according to claim 44, wherein said opaque conductive layer is formed by depositing an opaque conductive silicide layer.

56. The method according to claim 44, wherein said opaque conductive layer is formed by depositing an opaque conductive barrier metal layer.

57. The method according to claim 55, wherein said opaque conductive silicide layer is a tungsten silicide.

58. The method according to claim 55, wherein said opaque conductive silicide layer is a titanium silicide.

59. The method according to claim 55, wherein said opaque conductive silicide layer is a cobalt silicide.

60. The method according to claim 55, wherein said opaque conductive silicide layer is a molybdenum silicide.

61. The method according to claim 56, wherein said opaque conductive barrier metal layer is a TiN/W layer.

62. The method according to claim 56, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

63. The method according to claim 56, wherein said opaque conductive barrier metal layer is a WN_x layer.

64. The method according to claim 55, wherein said opaque conductive layer silicide layer is deposited by chemical vapor deposition.

65. The method according to claim 55, wherein said opaque conductive layer silicide layer is deposited by sputtering.

66. The method according to claim 56, wherein said opaque conductive barrier layer is deposited by chemical vapor deposition.

67. The method according to claim 56, wherein said opaque conductive barrier layer is deposited by sputtering.

68. The method according to claim 44, wherein said silicide is selectively removed by etching.

69. The method according to claim 44, wherein a ring portion of opaque conductive layer remains over an outer periphery of said photo-collection region.

70. The method according to claim 69, further including adding a light shield over a portion of said imager.

71. A processing system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor and including:

a substrate;

an array of pixel cells formed on said substrate, each of said cells including a photocollection region and at least one transistor wherein said transistor includes an opaque conductive layer deposited over the gate region of said transistor; and

signal processing circuitry on said substrate, wherein said circuitry is connected to said array.

72. The system according to claim 71, wherein said photo-collection region includes a photogate.

73. The system according to claim 71, wherein said opaque conductive layer is an opaque conductive silicide layer.

74. The system according to claim 71, wherein said opaque conductive layer is an opaque conductive barrier metal layer.

75. The system according to claim 73, wherein said opaque conductive silicide layer is a tungsten silicide.

76. The system according to claim 73, wherein said opaque conductive silicide layer is a titanium silicide.

77. The system according to claim 73, wherein said opaque conductive silicide layer is a cobalt silicide.

78. The system according to claim 73, wherein said opaque conductive silicide layer is a molybdenum silicide.

79. The system according to claim 74, wherein said opaque conductive barrier metal layer is a TiN/W layer.

80. The system according to claim 74, wherein said opaque conductive barrier metal layer is a WN_x/W layer.

81. The system according to claim 74, wherein said opaque conductive barrier metal layer is a WN_x layer.

82. The system according to claim 71, wherein said transistor is one or more of a reset transistor, a row select transistor, an amplifying transistor, a source follower transistor or a transfer transistor.

83. The system according to claim 71, wherein said transistor is a reset transistor.

84. The system according to claim 83, further comprising a transfer transistor to transfer charge from said photocollection region to said signal processing circuitry, wherein said transfer transistor includes an opaque conductive layer deposited over the gate region of said transistor.

85. The system according to claim 71, wherein said imager further includes a thin ring of opaque conductive layer formed over the outer periphery of said photogate.

86. The system according to claim 85, wherein said imager further includes a light shield formed over said imager such that said light shield does not cover a substantial portion of said photocollection region.